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6-BIT CMOS FLASH ADC USING TIQ COMPARATOR IN 0.250µM TECHNOLOGY

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ABSTRACT

The real universe signals are all analog in nature. Therefore, an analog to Digital converter is needed to transmit effectively the analog signals to digital. A low power and low voltage necessities are consideredprominent issues in the digital domain, as the channel length of MOSFET compresses lower than 0.25 sub-micron values. These trends flaunttopical challenges in ADC circuit design. This paper is an endeavour to contrive a flash analog to digital converter for low-power and high speed applications by integrating the threshold inverter quantization technique. Therefore, this paper is endured to the design and implementation of high speed, low voltage and low power flash analog to digital convertors. In this paper, a comparison of 6-bit flash ADC exercising TIQ comparator is manifested at 2.5 V and 3.3 V. A CMOS Flash ADC was schemed with 0.250 µm CMOS technology. Thefundamentalapproach to exercise this technique is to generate 2^n–1 different sized threshold inverter quantization comparators for an n-bit converter, ensuing that the fast data conversion speed enhances the operating speed and the elimination of ladder resistors directs asubstantial reduction in the power consumption. The schemed flash ADC facilitating TIQ is designed, exercising FAT tree encoder and simulated with the assistance of TANNER-EDA tool in 0.25 µm CMOS technology. The schemed ADC is appropriate for System-on-Chip (SoC) applications.

KEYWORDS: Flash ADC, TIQ Comparator, CMOS Technology, Fat Tree Encoder

INTRODUCTION

Analog to digital converters (ADCs) are of the most distinguishedcombined signal circuits. ADCs interface with the factual universe analog signals, the digital signal processing and computing world. The three essential parameters for an analog-to-digital converter are resolution, speed, and power consumption. These parameters cannot be changed once an ADC is designed.

This paper is an endeavour to contrive a flash analog to digital converter for low-power and high speed applications by integrating the threshold inverter quantization technique. Therefore, this paper is endured to the design and implementation of high speed, low voltage and low power flash analog to digital convertors. In this paper, a comparison of 6-bit flash ADC exercising TIQ comparator is manifested at 2.5 V and 3.3 V. A CMOS Flash ADC was schemed with 0.250 µm CMOS technology. The fundamental approach to exercise this technique is to generate 2^n–1 different sized threshold inverter quantization comparators for an n-bit converter, ensuing that the fast data conversion speed enhances the operating speed and the elimination of ladder resistors directs a substantial reduction in the power consumption. The schemed flash ADC facilitating TIQ is designed exercising FAT tree encoder and simulated with 0.25 µm CMOS technology utilising TANNER-EDA tool.

This paper explicates a CMOS flash ADC with an alternative technique for high speed and low voltage applications. This technique is popularised as Threshold Inverter Quantization (TIQ), as it uses the two cascading inverters

in voltage comparator. In this paper, the three provoking digital forces of low supply voltage, low power and high speed have been described in the design of a high-speed, low-voltage flash ADC (Uyttenhove *et* al., 2013). A general optimisation has been done to achieve the lowest power consumption possible for the 2.5 V V_{DD}, 555 MHz A/D converters Banik *et* al. (2011).The schemed ADC is appropriate for System-on-Chip (SoC) applications. This article is structured in the following manner: (1) introduction, (2) review of related work, (3) Theory of ADC, (4) brief about TIQ flash ADC, (5) design of ADC using TIQ technique, (6) simulation and results, (7) the conclusion.

REVIEW OF RELATED WORK

In this section, a review of related work pertained to designing of a low power TIQ based flash ADC has been presented. Khot *et* al. (2012) presented a design of a 3-bit 0.25µm CMOS Flash ADC, which is an ultrafast model based on TIQ comparator. Beased on their research, they concluded that the ADC based on TIQ comparators is highly suitable for not only the semiconductor technologies (below 100 nanometers) but also SoC applications. While Rajshekhar and Bhatt (2008) presented an ultrafast CMOS flash A/D converter design and performance. They used the featured A/D converter, which was designed in CMOS. The featured A/D converter utilised the Threshold Inverter Quantization (TIQ) technique to achieve high-speed in CMOS. They designed a 6-bit TIQ based flash A/D converter as per the parameter of 0.25 m standard CMOS technology, which occupies 0.013 mm^2area, dissipates 66.87mW of power at 2.5 V and operate with sampling rates up to 1 GSPS. They proposed an A/D converter, which is suitable for Systemon-Chip (SOC) applications in wireless products and otherultra-high speed applications.

Yoo *et* al. (2001a) presented a new power saving design method for CMOS flash ADC. The bisection method has been used so that only half of the comparators should work in every clock cycle with NMOS and PMOS as switches. With the help of this exercise, they have demonstrated a 6-bit flash ADC working at 3.3V voltage supply and 200 MHz sampling rate and found that the power consumption of proposed circuit is only 40.75mW with HSPICE simulation. Comparing to a traditional flash ADC, this bisection method may mitigate the power consumption to 43.18%. Tsai (2004) presented the design of an 8-bit FLASH Analog to Digital (A/D) Converter with Threshold Invert Quantization (TIQ) Comparators. They used the speed of this ADC 787.78 Mbps and the power consumption at 800mW. All individual blocks were designed and simulated by using T-spice with 0.18 2m CMOS Technology.

Rames and Gunavathi (2007) proposed a 4-bit, 1.8V Flash ADC design exercising the CMOS Linear Tunable Transcoductance Element Comparator with 500nm technology. They have generated the Reference voltages systematically sizing the transistors of the comparators. Kulkarni *et* al. (2010) proposed a 4-bit flash ADC converter for low power SoC applications. They used CMOS inverter as a comparator and by altering the ratio of width and length of the channel. For detecting the input Analog signals, the switching threshold of the CMOS inverter has also been adjusted. The simulation results shown that this proposed ADC can reduce the power consumption about 78%. Mohan and Ravisekhar (2014) proposed an efficient, low power encoding scheme intended for flash analog to digital convertor. They used CMOS inverter as a comparator for keping the high speed with low power dissipation. They proposed ADC is designed using 90n m technology in 1.2 V power supply using HSPICE tool.

THEORY OF ADC

The various types of ADCs have been studied in the literature, most notably are Flash ADC, Sigma delta ADC, Ramp counter ADC and Successive approximation ADC. However, the flash ADC architecture has been widely studied. It

is faster due to its parallel architecture. That's why; it is also called as parallel ADC. It is exercised by comparing the analog signal (the input voltage) to a reference voltage that is maximum value achieved by the analog signal. For a ready reference the same can be understood by the following illustration. Suppose, the reference voltage is about 5 volts, means the peak of the analog signal will be 5 volts. When, the input signal will reach to 5 volts on an 8-bit ADC, we will get the maximum possible value on the ADC output i.e. 255 (11111111). Then, the reference voltage can be lowered through the register network and other comparators can be added to compare the analog signal (the input voltage) with other values (Khot *et* al., 2012).

TIQ FLASH ADC

The flash ADC advances the threshold inverter quantization (TIQ) technique for high speed, low power using standard CMOS technology and compatible with microprocessor fabrication(Rames and Gunavathi, 2007; Khot *et* al., 2012). The block diagram of the TIQ flash ADC has been presented in figure 1.

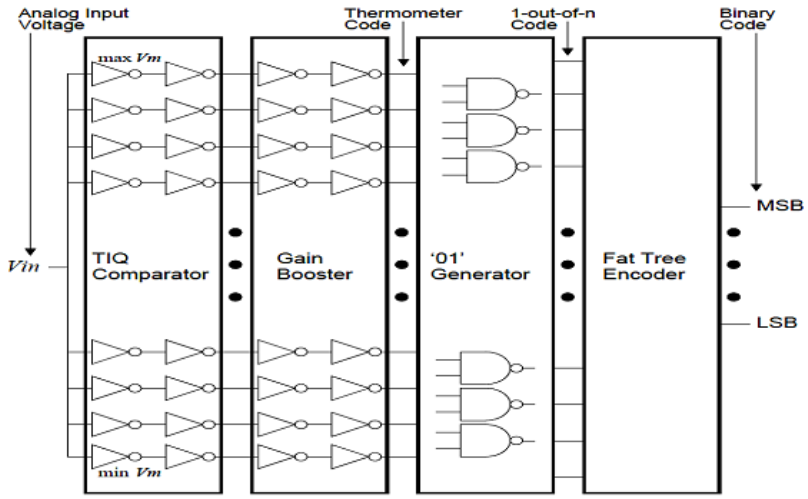


Figure 1: Block Diagram of ADC (Adopted from Banik*et* al., 2011)

"The voltage comparators compare the input voltage with internal reference voltages, which are determined by the transistor sizes of the inverters." Therefore, the resistor ladder circuit used in a conventional flash ADC is not required in the design of TIQ Flash ADC (Rames and Gunavathi, 2007; Mavani and Nandurbarkar, 2014).

For generating a high speed CMOS flash ADC comparator, Threshold inverter quantization (TIQ) is considered and utilised as a unique method. A key parameter to differentiate between differential comparator and the TIQ comparator is; the supply of their reference voltages. The differential comparator utilises the external reference voltage V_r using a resistor ladder circuit. The V_r directly depends on a resistor tap position. However, on the basis of the transistor size, the TIQ comparator sets the V_m internally as the built-in reference voltage. The TIQ based ADC has individual comparators in all different sizes in contrast to the conventional flash ADC, which uses the identical in size comparators. For developing an n-bit flash TIQ based ADC, one must find 2^n-1different inverters, and each has different V_m value. And one must arrange them in the order of their V_m value (Khot *et* al., 2012).

Rames and Gunavathi (2007) stated that the TIQ comparator is a pure inverter circuit; it is faster and simpler than the differential comparator. It has the several advantages, most notably:

- The clock signals, switches, or coupling capacitors are not necessary in the TIQ comparator when comparing the input voltage,
- Utilizing standard digital CMOS process, it enables the TIQ comparator as a highly suitable for SOC applications
- Only two transistors are required in between the power supply rails.

The advanced CMOS technology with below 1.0V voltage power supply and below 0.1μm feature size makes possible the realization of a TIQ comparator realisation (Yoo *et* al., 2002).

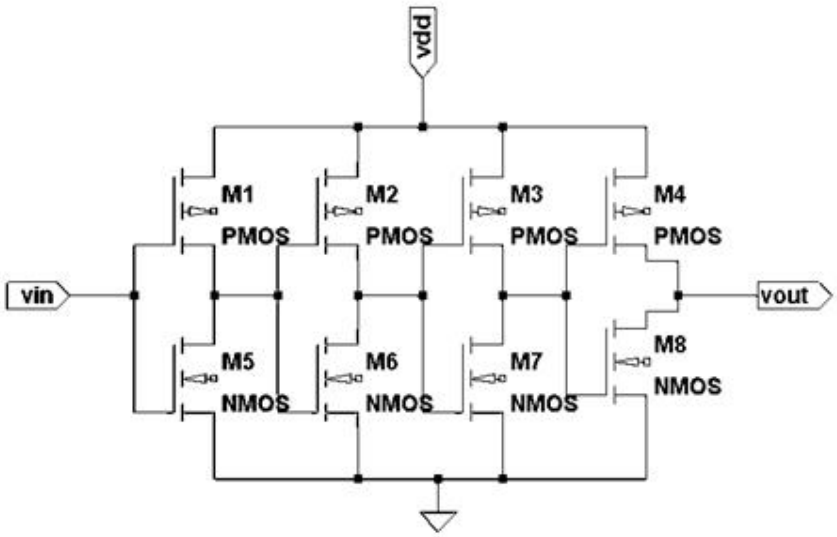


Figure 2: TIQ Comparator (Adopted from Ghai 2007)

Kulkarni *et* al. (2010) stated that there are some basic problems with conventional comparator structures in Analog to Digital designs. Most notably: a large transistor area for higher accuracyis required, DC bias requirement, charge injection errors, meta stability errors, high power consumption, and a resistor or capacitor array requirement. Yoo *et* al. (2001) suggested that these problems can be eliminated by using "Threshold Inverter Quantizer". The TIQ technique has several advantages: simpler voltage comparator circuit, faster voltage comparison speed, elimination of resistor ladder circuit, not require coupling capacitors for the voltage comparison, switches and clock signal. It is highly suitable for futurisms technology development. It is going to be smaller feature size and requires the lower voltage of supply

The TIQ comparator id a very sensitive to power supply noise and have a single ended input (Banik *et* al., 2011). The reference voltages are changed when there is a noise in the power supply voltage. To overcome this problem the CMOS Linear Tunable Trans conductance Element (CMOS-LTE) comparator has been proposed, which uses the TIQ comparator concept for the generation of reference voltages (Iyappan *et* al. 2009).

DESIGN OF ADC USING TIQ TECHNIQUE

The design of a flash ADC using TIQ technique is shown in Figure1.

Design of TIQ Comparator Section

Ali and Choi (2001) presented a design method and the automation of the comparator circuit layout generation for a flash A/D converter. The 2^n- 1 comparators are needed for TIQ based ADCs, each one should differ from all others.

The optimal design method proposed by Ali and Choi (2001) for the TIQ comparator improvises the linearity of the A/D converter against the variation of CMOS process.

The TIQ comparator circuit consists of four cascaded inverters, as shown in Figure 2. There are four inverters in cascade in order to provide a sharper switching for the comparator and also provide a full voltage swing. The comparator comprises the PMOS and NMOS transistors of the same size, but they differ for different comparators. They depend upon the switching voltage they are designed for. The mathematical expression used for deciding these switching voltages is given as:

$$V_{switching} = \frac{\sqrt{\frac{\mu_p W_p}{\mu_n W_n}}\left(V_{DD} - \left|V_{tp}\right|\right) + V_{tn}}{1 + \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}}$$

(Adopted from Lee *et* al., 2002)

Where,

W_p= PMOS width,

W_n= NMOS width,

V_{DD}= Supply voltage,

V_{tn}= NMOS threshold voltage,

V_{tp}= PMOS threshold voltage,

μ_n= Electron mobility,

μ_p= Hole mobility,

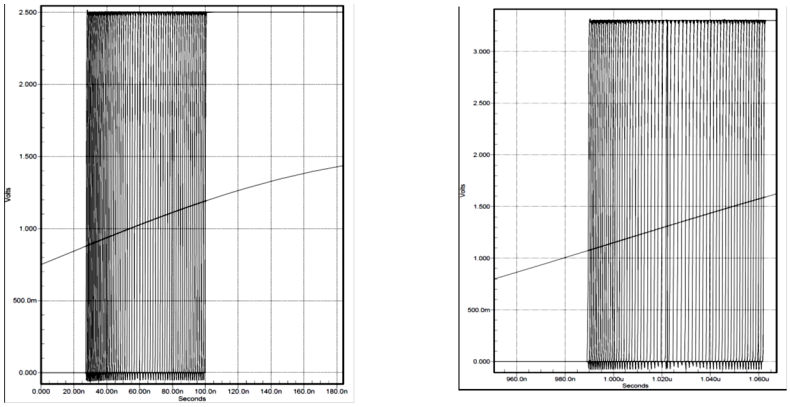
Assuming that PMOS length = NMOS length.

The comparison voltage ($V_{m)}$ can be changed by modulating the sizes of used transistor. However, switching threshold voltage (V_m) is internally set by the TIQ comparator. The built-in reference voltage depends on the size of the used transistor. The TIQ based ADC used individual as well as all different sized comparators as compared to the conventional flash ADC. To develop an n-bit flash TIQ based ADC, individual needs to have 2^n - 1 different inverters and each inverter must have different V_m value, and individual must order them in the order of their V_m value. For a 6-bit ADC, 63 individual TIQ comparators are needed (Ghai *et* al., 2007; Lee *et* al., 2002; Khot *at* al., 2012).

As the input Analog voltage increases, the comparators start turning on in succession. Thus, thermometer code at the output of the comparators would be received. “The point where the code changes from one to zero is the point where the input signal becomes smaller than the respective comparator reference voltage levels.” This is known as thermometer code encoding (Madhumati *et* al., 2009).

Result of a TIQ Comparator

For n-bit Flash ADC we require 2^n-1 TIQ comparators, so we require 63 for 5-bit flash ADC design. This is achieved by varying the widths of PMOS and we get different switching voltages. The output result of the 6-bit TIQ comparator section is shown in the Figure 3.



(a) (b)

(a) VDD=2.5V (b) VDD=3.3V

Figure 3: Switching of Various Comparators for6- bit TIQ Flash ADC

Design of 1 Out of N Code Generator

The output of the comparators in a flash ADC is a thermometer code. This thermometer code is converted to a binary code using an encoder in two steps. The thermometer code is first converted into a 1-out-of-n code using 1-out of n code generators, which generates a '01' code. This '01' code is converted into a binary code using a fat tree encoder (Chauhan*et* al., 2011).

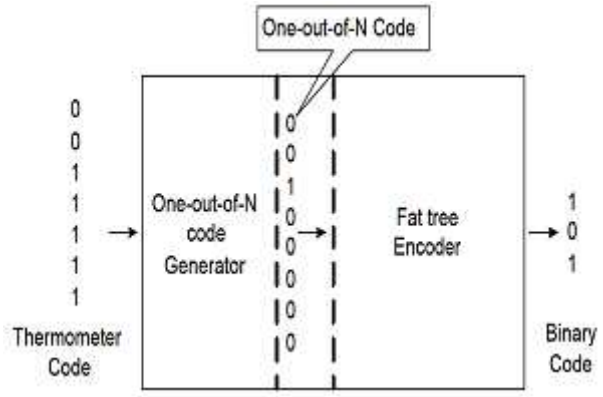


Figure 4: Two Stage Fat Tree TC-BC Encoder(Adopted from Lee *et* al., 2002a)

Fat Tree Encoder

For designing the ultra-high speed flash ADCs, the thermometer code-to-binary code encoders have become necessity. The fat tree thermometer code-to- binary code encoder has been presented in this paper, which is highly adoptable for designing the ultra-high speed flash ADCs.

The fat tree encoder is considered to be better than the ROM encoder in terms of speed and power supply for the CMOS flash ADC. By using the fat tree encoder, the speed can be improved by almost a factor of 2, which demonstrates

that the fat tree encoder is an effective solution for the bottleneck problem in ultra-high speed ADCs (Chauhan *et* al., 2011; Lee *et* al., 2002).

The TC (thermometer code)-to-BC(binary code) encoding is carried out in two stages in the fat tree encoder: the first stage converts the thermometer code to one-out-of-N code (Chauhan *et* al., 2011). This is shown in Figure 4. The one-out-of-N code is same as an address decoder output. This code conversion is done inNbit parallel using the gates. The second stage converts the one-out-of-N code to binary code using the multiple trees of OR gates shown in Figure 5 for 4-bit case.

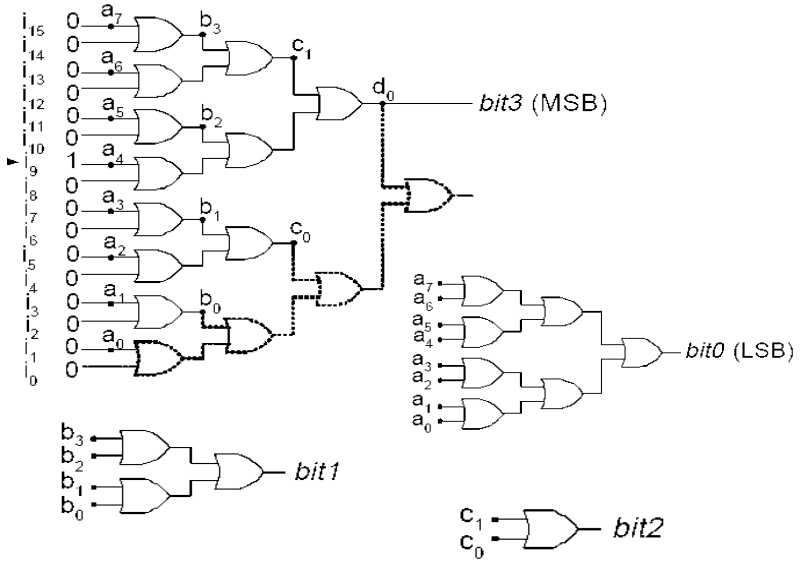


Figure 5: Fat Tree Encoder for 4-bit (Adopted from Chauhan et al., 2011)

Design Steps

- Design a minimum size inverter and verify the threshold voltage value of the midpoint quantizer, Qn, using the HSPICE circuit simulator by substituting BSIM3 (Level 49) spice model test parameters obtained from a vendor for a specific technology. Note that the channel length is kept at the minimum value during the entire design process.
- Estimate a safe analog input voltage range as follows: *Analog range = Vdd - (VTN + | VTP|)*, where *VTN* and *VTP* are the threshold voltages for large NMOS and PMOS devices, namely the VTHO value from the model parameter data set used during the entire design process.
- Calculate the LSB value as follows: *LSB = Analog range/ 2^n*.

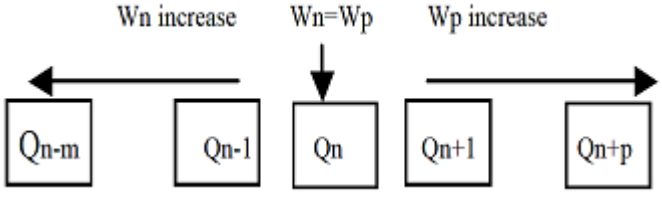
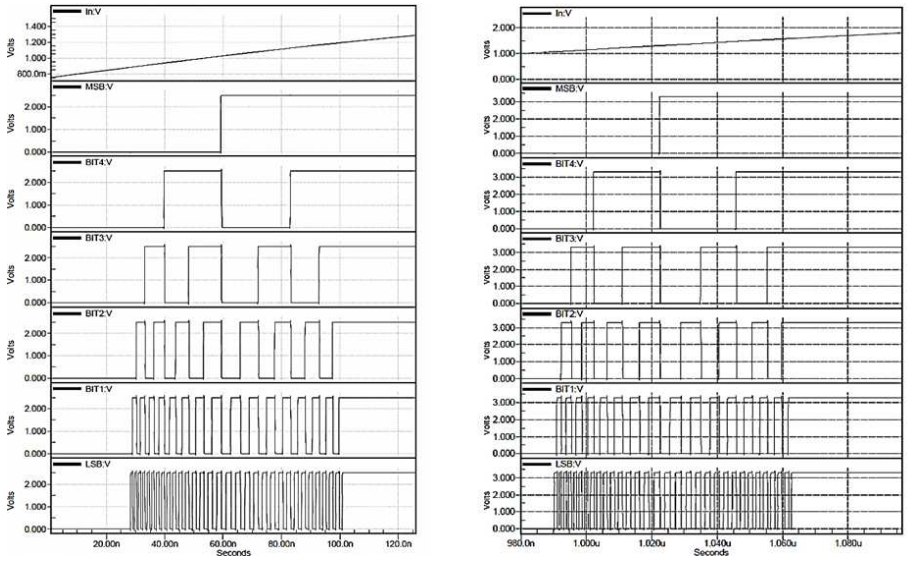


Figure 6: Block Diagram of a Design Process (Adopted from Kulkarni *et* al. 2010)

- Calculate the ideal threshold points for each quantizer (Qn-m … Qn+p) accordingly, assuming the midpoint value for Qn is in the center.
- Run the HSPICE simulator to obtain the corresponding closest possible channel widths. Note that for the quantizers of Qn+1 … Qn+p), the so-called PMOS side, (W/L)n is kept at the minimum value, but only the channel widths of the PMOS transistors are changed to minimise the current flow during the transition of VTC (metastable region). This process is applied to the NMOS side in the opposite way (Kulkarni *et* al., 2010)

SIMULATION AND RESULTS

TANNER-EDA tools were exercised to simulate the schematic circuit for designing the flash ADC in order to btain the results. After simulating the schematic circuit by employing the T-Spice tool of TANNER-EDA tool, the outputs of 6-Bit flash ADC has been notified and the same has been presented in Figure 7



(a) **(b)**

Figure 7: Output of 6-bit TIQ Flash ADC (a) V_{DD}=2.5V (b) V_{DD}=3.3V

CONCLUSIONS

A **s**imple and fast flash ADC architecture that uses two cascaded CMOS inverters as a comparator, called threshold inverter quantization (TIQ) technique has been proposed and fastest encoder called a fat tree encoder has been used. The results are summarised in the following table. The design and simulation results of6-bit Flash ADC using 0.25µm technology have been presented using TANNER- EDA tools. The power supply voltage given is 2.5 V and 3.3V. However, the circuit should be portable to smaller feature size CMOS technologies with lower supply voltages. The result is summarised in following table.

Table 1

Resolution (No. of Output Bits)	6-Bit	
CMOS Technology	0.250 µm	
Transistor count	1928	
Power Supply(V_{DD})	2.5V	3.3V
Max Speed(MSPS)	500	565
Average Power Consumed(mW)	22.28	45.03

Table 1: Contd.,		
Vm Range(Input Dynamic Range)	0.85V-1.2V	1.1V-1.6V
Vm Distance(V_{FSR}) (V)	0.35	0.5
V_{LSB}	0.00564	0.00806
Input signal frequency	1MHz	

Moreover, it is worth indicating that the schemed ADC in this paperis a clock less circuitry, which is also a logic for the lowered the power consumption. However, it has been further planned to integrate the comparator using latest CMOS technology. Thus, an ADC which is functional at Nano scale CMOS technologies has been successfully designed and demonstrated. The challenges in designing high-speed CMOS flash ADCs are optimising the speed and power, static and dynamic offset reduction, calibration, and low supply voltage operation. The design is targeted for applications such as high-speed serial links and UWB that require 4 bits of resolution at multi-GHz speeds.

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